IN THE CLAIMS:

1. (original) A semiconductor memory, comprising:

a memory cell array including a plurality of blocks separated in column direction every M word lines, the separated blocks sharing N+1 virtual ground wires, which are selectively subject to ground-connection in response to address operation and N main bit lines, each of which is placed between the adjacent two of the virtual ground wires and selectively subject to sensing-connection, the separated blocks being adjacent one after another in column direction with the adjacent two in symmetric relationship around an imaginary line separating the adjacent two blocks,

each of the separated blocks including diffusion wires which are equi-distant one fourth the virtual ground wires are, and memory cells in M rows and in 4 N columns grouped as a memory cell unit,

each of the separated blocks including, on one end side of the diffusion wires, a bit select line and, per each of the memory cell units, three bit column select transistors, which use a middle diffusion wire and the adjacent two diffusion wires of a set of diffusion wires provided for the memory cell unit as drains or sources, and the bit column select line as gates, each of the three bit column select transistors having diffusion layer connected to one of the main bit lines,

each of the separated blocks including, on the other end side of the diffusion wires, a ground select line and, per each of the memory cell units, three ground select transistors, which use a boundary diffusion wire of the set of diffusion wires and the adjacent two

diffusion wires as drains or sources, and the ground select line as gates, each of the three ground select transistors having diffusion layer connected to one of the virtual ground lines,

inter-block bit wires, each connecting the middle diffusion wire for one of the memory cell units of first block of the separated blocks and the middle diffusion wire for one of the memory cell units of the adjacent second block lying on the other end side of the diffusion wires of the first block,

the first block and the adjacent second block having halves of the inter-block bit wires, respectively,

inter-block ground wires, each connecting the boundary diffusion wire for the one memory cell unit of the first block and the boundary diffusion wire for the one memory cell unit of the adjacent third block lying on the one end side of the diffusion wires of the first block,

the first block and the adjacent third block having halves of the inter-block ground wires, respectively.

2. (original) The semiconductor memory as claimed in claim 1, wherein each of the inter-block bit wires interconnects the other ends of the middle diffusion wires of the first block and the adjacent second block, and wherein each of the inter-block ground wires interconnects one ends of the boundary diffusion wires of the first block and the adjacent third block.

3. (original) The semiconductor memory as claimed in claim 1, wherein each of the inter-block bit wires interconnects one ends of the middle diffusion wires of the first block

and the adjacent second block, and wherein each of the inter-block ground wirers interconnects the other ends of the boundary diffusion wires of the first block and the adjacent third block.

4. (original) The semiconductor memory as claimed in claim 3, wherein the inter-block bit wires and the inter-block ground wires are formed within a different wiring layer from where the main bit lines and the virtual ground wires are formed, and wherein the inter-block bit wires and the inter-block ground wires are connected via connectors to the diffusion wires.

5. (currently amended) The semiconductor memory as claimed in claim ~~any one of claims~~ 1 ~~to 4~~, wherein the main bit lines are formed within a different wiring layer than a wiring layer where the virtual ground wires are formed.

6. (original) The semiconductor memory as claimed in claim 1, including at least one of dummy bit select block and dummy ground select block lying adjacent and next to one of the fist stage block and a last stage block of plural blocks, said dummy bit and ground select blocks being free from memory cells.

7. (original) The semiconductor memory as claimed in claim 6, wherein the dummy bit select block includes a bit column select transistor having drain or source connected to one of the inter-block bit lines, and gate connected to the bit select line, and wherein the dummy bit select block includes, per each of the memory cell units, a transistor or dummy diffusion layer connected to one of the inter-block bit lines and being electrically equivalent to three diffusion wires.

8. (original) The semiconductor memory as claimed in claim 6, wherein the dummy ground select block includes a ground select transistor having drain or source connected

to one of the inter-block ground wire, and gate connected to the ground select line, and wherein the dummy ground select block includes, per each of the memory cell units, a transistor or dummy diffusion layer connected to one of the inter-block ground line and electrically equivalent to the diffusion line.

9. (original) A semiconductor memory comprising:

a memory cell array including blocks separated every M word lines in column direction, the blocks including a plurality of main bit lines, which are subject to precharge and ground-connection,

the blocks being arranged one after another in column direction, with the adjacent two thereof in symmetrical relation about a line separating them,

the blocks including diffusion wires, which are distant one half the main bit lines are, and a plurality of memory cells grouped into a memory cell unit in M rows and in two columns, the memory cells using the adjacent two diffusion wires as drain or source and the M word lines as gates,

the blocks including diffusion layer connected to one of the main bit lines and three column select transistors, which use the diffusion wire corresponding to one of the main bit lines and the adjacent diffusion wires as drain or source and a first and a second column select lines as gate,

the blocks include halves of an inter-block bit line, which interconnect the diffusion lines corresponding to one of the main bit line between one block and the adjacent blocks.

10. (cancelled)